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Clean Version of Pending Claims

CIRCUITS WITH A TRENCH CAPACITOR HAVING MICRO-ROUGHENED SEMICONDUCTOR SURFACES
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Claims 17-40, as of March 22, 2000 (Date Response to First Office Action filed).

17. A memory cell, comprising:

a lateral transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region;

a trench capacitor formed in a trench and coupled to the first source/drain region; and

wherein the trench capacitor includes a polycrystalline semiconductor plate formed in the trench that is coupled to the first source/drain region, a second plate formed by the substrate with a surface of the substrate in the trench roughened by etching a polycrystalline semiconductor material on the surface of the substrate, and an insulator layer that separates the polycrystalline semiconductor plate from the roughened surface of the substrate.

18. The memory cell of claim 17, wherein the polycrystalline semiconductor plate comprises polysilicon.

19. The memory cell of claim 17, wherein the second plate comprises a heavily doped p-type silicon substrate.

20. The memory cell of claim 17, wherein the second plate of the trench capacitor comprises the substrate with an anodic-etch-roughened surface.

21. The memory cell of claim 17, wherein the second plate of the trench capacitor comprises the substrate with a phosphoric-acid-etch-roughened surface.

22. A memory cell, comprising:

a vertical transistor formed outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region that are vertically aligned;

wherein a surface of the first source/drain region is roughened by etching a polycrystalline semiconductor material on a surface of the first source/drain region; and

a trench capacitor with a plate that is formed in a trench that surrounds the roughened surface of the first source/drain region of the transistor.

23. The memory cell of claim 22, wherein the first source/drain region comprises single crystalline silicon with a layer of polysilicon formed on its surface in the trench, wherein the layer of polysilicon includes a phosphoric-acid-etch-roughened surface.

24. The memory cell of claim 22, wherein the first source/drain region comprises single crystalline silicon with a layer of polysilicon formed on its surface in the trench, wherein the layer of polysilicon includes an anodic-etch-roughened surface.

25. The memory cell of claim 22, wherein the plate comprises polysilicon.

26. A memory device, comprising:

an array of memory cells, each memory cell including an access transistor that is coupled to a trench capacitor wherein a first plate of the trench capacitor includes a micro-roughened surface of porous polysilicon and a second plate of the trench capacitor disposed adjacent to the first plate;

a number of bit lines that are each selectively coupled to a number of the memory cells at a first source/drain region of the access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

27. The memory device of claim 26, wherein the comprises a layer of polysilicon formed on a surface in the trench and includes a phosphoric-acid-etch-roughened surface.

28. The memory device of claim 26, wherein the comprises a layer of polysilicon formed on a surface in the trench and includes an anodic-etch-roughened surface.

29. The memory device of claim 26, wherein the second plate comprises polysilicon.

30. The memory device of claim 29, wherein the access transistor comprises a lateral transistor that is coupled to the second plate of the trench capacitor.

31. A memory cell, comprising:

a lateral transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region; and

a trench capacitor formed in a trench and coupled to the first source/drain region;

wherein the trench capacitor includes a polysilicon plate formed in the trench that is coupled to the first source/drain region, a second plate formed by the substrate with a surface of the substrate in the trench roughened by etching a polysilicon material on the surface of the substrate, and an insulator layer that separates the polysilicon plate from the roughened surface of the substrate.

32. The memory cell of claim 31, wherein the second plate comprises a heavily doped p-type silicon substrate.

33. A memory cell, comprising:

a lateral transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region; and

a trench capacitor formed in a trench and coupled to the first source/drain region;

wherein the trench capacitor includes a polysilicon plate formed in the trench that is coupled to the first source/drain region, a second plate formed by the substrate in the trench, the second plate having a phosphoric-acid-etch-roughened surface or an anodic-etch-roughened surface, and an insulator layer that separates the polysilicon plate from the phosphoric-acid-etch-roughened surface or anodic-acid-etch-roughened surface of the substrate

34. A memory cell, comprising:

a vertical transistor formed outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region that are vertically aligned, wherein the first source/drain region comprises single crystalline silicon with a layer of polysilicon formed on its surface; and

a trench capacitor with a plate that is formed in a trench that surrounds a roughened surface of the first source/drain region of the transistor;

wherein the roughened surface of the first source/drain region of the transistor is anodic-etch-roughened or phosphoric-acid-etch-roughened.

35. A memory device, comprising:

an array of memory cells, each memory cell including an access transistor that is coupled to a trench capacitor wherein a first plate of the trench capacitor includes a micro-roughened surface of porous polysilicon a second plate of the trench capacitor is disposed adjacent to the first plate, further wherein the micro-roughened surface of porous polysilicon is anodic-etch-roughened or phosphoric-acid-etch-roughened;

a number of bit lines that are each selectively coupled to a number of the memory cells at a first source/drain region of the access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

36. The memory device of claim 35, wherein the access transistor comprises a lateral transistor that is coupled to the second plate of the trench capacitor.

37. The memory cell of claim 31, wherein the first source/drain region is P-doped or N-doped.

38. The memory cell according to claim 33, wherein the first source/drain region is N-doped or P-doped.

39. The memory cell according to claim 34, wherein the single crystalline polysilicon is P-doped or N-doped.

40. The memory cell according to claim 35, wherein the portion of the access transistor is P-doped or N-doped.